CLAIMS

[1] A cache memory system comprising:

a condition generation unit operable to generate a condition concerning a state of a processor;

a judgment unit operable to judge whether or not a current state of the processor satisfies the condition;

an address generation unit operable to generate an address to be manipulated; and

a manipulation unit operable to manipulate a cache using the address generated by said address generation unit, when said judgment unit judges that the condition is satisfied.

[2] The cache memory system according to Claim 1,

wherein said condition generation unit is operable to generate a new condition in the case where said judgment unit judges that the condition is satisfied.

[3] The cache memory system according to Claim 2,

wherein said condition generation unit is operable to generate a condition concerning a value of a specific register, within the processor.

[4] The cache memory system according to Claim 3,

wherein the specific register is a program counter.

[5] The cache memory system according to Claim 2,

wherein said condition generation unit is operable to generate, as the condition, one of memory access within a specific address range and memory access outside of the specific address range.

[6] The cache memory system according to Claim 1,

wherein said condition generation unit is operable to generate,

as the condition, execution of a specific instruction by the processor.

[7] The cache memory system according to Claim 2,

wherein said condition generation unit is operable to generate the new condition by performing a specific calculation on a current condition.

[8] The cache memory system according to Claim 7,

wherein said condition generation unit is operable to:

generate a memory access address as the condition; and

generate the new condition by adding a constant to the current condition in the case where said judgment unit judges that the condition is satisfied.

[9] The cache memory system according to Claim 8,

wherein the constant is one of: an increment value or decrement value in a post-increment load/store instruction executed by the processor; and a difference value of addresses in two load/store instructions executed by the processor.

[10] The cache memory system according to Claim 1,

wherein said condition generation unit is operable to generate plural conditions, and

said judgment unit is operable to judge whether or not all of the plural conditions are satisfied.

[11] The cache memory system according to Claim 1,

wherein said condition generation unit is operable to generate plural conditions, and

said judgment unit is operable to judge whether or not any of the plural conditions are satisfied.

[12] The cache memory system according to any of Claim 1 through Claim 3,

wherein said manipulation unit includes:

a data judgment unit operable, in the case where said judgment unit judges that the condition is satisfied, to judge whether or not data corresponding to the address generated by said address generation unit is stored in the cache;

a selection unit operable to select a line within the cache memory in the case where it is judged that the data is not stored;

a write back unit operable to perform a write back from the selected line when the selected line is valid and dirty;

a transfer unit operable to transfer, from a memory to the selected line after the write back, the data corresponding to the address; and

a registration unit operable to register the address as a tag, to the selected line.

[13] The cache memory system according to any of Claim 1 through Claim 3,

wherein said manipulation unit includes:

a data judgment unit operable, in the case where said judgment unit judges that the condition is satisfied, to judge whether or not data corresponding to the address generated by said address generation unit is stored in the cache;

a selection unit operable to select a line within the cache memory in the case where it is judged that the data is not stored;

a write back unit operable to perform a write back from the selected line when the selected line is valid and dirty;

a registration unit operable to register the generated address as a tag, to the selected line, without transferring data from a memory to the selected line.

[14] The cache memory system according to any of Claim 1 through Claim 3,

wherein said manipulation unit includes:

a data judgment unit operable, in the case where said judgment unit judges that the condition is satisfied, to judge whether or not data corresponding to the address generated by said address generation unit is stored in the cache;

a selection unit operable, in the case where it is judged that the data is stored, to select a line, within the cache memory, in which the data is stored;

a write back unit operable to perform a write back from the selected line when the selected line is valid and dirty.

[15] The cache memory system according to any of Claim 1 through Claim 3,

wherein said manipulation unit includes:

a data judgment unit operable, in the case where said judgment unit judges that the condition is satisfied, to judge whether or not data corresponding to the address generated by said address generation unit is stored in the cache;

a selection unit operable, in the case where it is judged that the data is stored, to select a line, within the cache memory, in which the data is stored;

an invalidation unit operable to invalidate the selected line.

[16] The cache memory system according to any of Claim 1 through Claim 3,

wherein said manipulation unit includes:

a data judgment unit operable, in the case where said judgment unit judges that the condition is satisfied, to judge whether or not data corresponding to the address generated by said address generation unit is stored in the cache;

a selection unit operable, in the case where it is judged that the data is stored, to select a line, within the cache memory, in which the data is stored;

a change unit operable to change an access order of the selected line in order information indicating an order in which lines are accessed.

[17] The cache memory system according to any of Claim 12 through Claim 16,

wherein said condition generation unit is operable to generate a memory address as the condition, and

said manipulation unit further includes

an adjustment unit operable, in the case where the memory address generated by said condition generation unit indicates a point midway through a line, to generate an address by adjusting so that one of a starting point of the line, a starting point of a next line, and a starting point of an immediately preceding line is indicated.

[18] A cache memory control method comprising:

a condition generation step of generating a condition concerning a state of a processor;

a judgment step of judging whether or not a current state of the processor satisfies the condition;

an address generation step of generating an address to be manipulated; and

a manipulation step of manipulating a cache using the address generated in said address generation step, when it is judged in said judgment step that the condition is satisfied.